A Built-In I_{DDQ} Testing Circuit*

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Abstract:

Although I_{DDQ} testing has become a widely accepted defect detection technique for CMOS ICs, its effectiveness in very deep submicron technologies is threatened by the increased transistor leakage current. In this paper, a built-in I_{DDQ} testing circuit is presented, that aims to extend the viability of I_{DDQ} testing in future technologies and first experimental results are discussed.

1. Introduction

Quiescent current (I_{DDQ}) testing is a well established technique for defect detection in CMOS ICs. However, the effectiveness of I_{DDQ} testing is threatened by the fact that technology evolution leads to a remarkable increase of the intrinsic (defect-free) quiescent current (here after called background current, I_B) [1-2] while in parallel the defective currents (I_{DEF}) that are required to be detectable are decreased [3]. In addition the number of transistors in a single chip is increased rapidly resulting in a further increase of the background current and a further decrease in the gap between I_B and I_{DEF}. Then, considering that the fluctuations in the value of I_B are increased due to manufacturing process variations, the application of I_{DDQ} testing using a single threshold for discrimination between defect free and defective circuits will either lead to yield loss or reduced fault coverage.
Many I_{DDQ} testing approaches have been proposed in the open literature [1, 4]. Recently, a new I_{DDQ} testing technique was presented in [5] that is based on background current compensation. In this work, exploiting this approach, we present a new built-in I_{DDQ} testing circuit to confront background current related problems and perform I_{DDQ} testing using a single reference voltage for defective circuit detection. The paper is organized as follows: in section 2 the proposed circuit is presented while in section 3 experimental results are provided from a fabricated demonstrator, finally the work is concluded in section 4.

2. The proposed I_{DDQ} test circuit

The general idea under the proposed I_{DDQ} testing approach is presented in Fig. 1. A tail transistor MN_T is added between the circuit under test (CUT) and the ground supply (Gnd) (equivalently a head transistor at the side of the power supply V_{DD} could be used). This transistor is biased with a proper voltage V_{bias} so that in the defect free case the voltage V_{V_Gnd} at the virtual ground node (V_Gnd) is less than a reference voltage V_{REF}, while in the defective case this voltage will be higher than V_{REF} due to the lower resistance of the CUT in the presence of the fault. Then a comparator (COMP) could be used to discriminate between defect free and defective cases. In this topology the CUT and the tail transistor act as a current to voltage converter, where the CUT is biased with a background current I_B that is controlled by V_{bias}. The bias voltage V_{bias} can be generated in a trivial way using an injection current I_{INJ} and a current mirror. Note that another transistor MN_G is introduced in the above scheme to switch between the normal and the test mode of operation utilizing the test enable signal *T_ENB* (active "low").

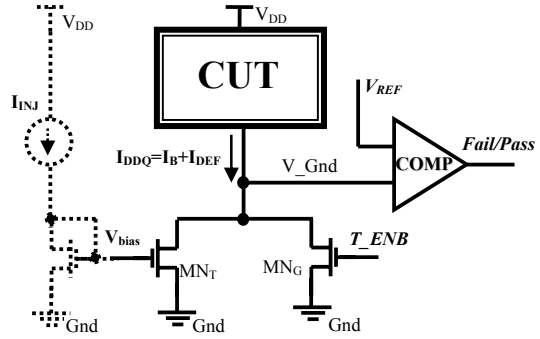

Figure 1. An I_{DDQ} testing scheme

However, the background current I_B of the CUT is influenced by process and temperature variations. Thus the injection current I_{INJ} must be accordingly adjusted in order to avoid a reduced fault coverage or a yield loss. Considering these two parameters, it is obvious that we need a mechanism that dynamically adjusts I_{INJ} to these fluctuations. The adopted approach is to partition the CUT into two subcircuits (sub-CUT_L and sub-CUT_R) as illustrated in Fig 2. Then the background current of the left subcircuit is used as injection current for the testing of the right subcircuit and vice-versa. Since in each case the background and the injection currents are influenced by the same process and temperature variations in the CUT, the I_{DDQ} testing process turns to be independent of these two factors. According to the block diagram of Fig. 2, a single Current Mirror Amplifier (CMA) and a Comparator (COMP) are used to test both subcircuits.

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During the I_{DDQ} testing of sub-CUT_R, only the signal *Test_sub-CUT_R* is "high". Then the background current I_{BL} of sub-CUT_L is used as injection current at the *INJCT* port of the CMA for the generation of the bias current $I_{BIAS\_R}=\beta_L I_{BL}$, at the *BIAS* port of the CMA, to test sub-CUT_R (β_L is the current gain of the mirror). The bias current to test sub-CUT_L is generated in the same way using the background current of sub-CUT_R as injection current for the CMA setting only *Test_sub-CUT_L* to "high". Note that β_L and β_R can take values lower than unit. Thus, the I_{DDQ} test process is divided into two successive phases; the first phase where sub-CUT_L provides the injection current and sub-CUT_R is the circuit under test and the second phase where sub-CUT_R provides the injection current and sub-CUT_L is the circuit under test (see Fig. 3).

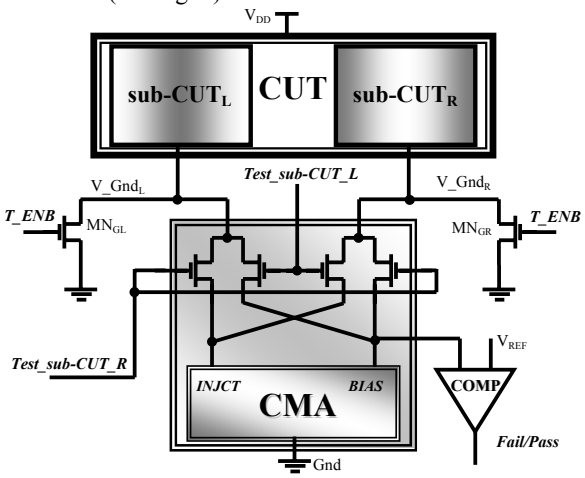

Figure 2. The proposed I_{DDQ} testing architecture

In Fig. 4 an efficient ground supply partitioning technique is illustrated in order to form the two subcircuits and provide equivalent dependence of both background (injection) currents on process and temperature variations. Two independent ground rails (V_Gnd_L and V_Gnd_R) are interdigitated inside the CUT to provide the ground supply. The parts of the CUT with common ground rail constitute a subcircuit. Note that according to this scheme the number of partitions is reduced to only two compared to the huge number of partitions discussed in [6] for I_{DDQ} testing.

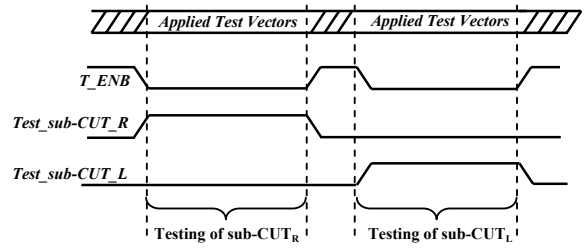

Figure 3: I_{DDQ} testing signals' waveforms

However the background current also depends on the applied test vector and the size of each subcircuit. In order to take into account these dependences a Programmable Current Mirror/Amplifier (PCMA) has been adopted, that is a current mirror with programmable current gain β. For each test vector of the I_{DDQ} test set the background currents of the two subcircuits are estimated by simulations [7] and the required current gain β is determined. This approach is applicable since the cardinality of a test set for I_{DDQ} testing is relatively small [8] and thus the simulation phase will be not a time consuming process (beside this, it is performed only once). Moreover, selecting suitably the test vectors, based on static power analysis [9], we can further reduce the background current variations from test vector to test vector and group together the test vectors for which the corresponding background currents present neighboring values. Then each group of test vectors is accompanied by the identification of the proper state of the PCMA that must be activated. Possible differences between the simulated and the actual, in the field, background currents I_B of the CUT do not invalidate the method since these variations affect in the same way both background currents.

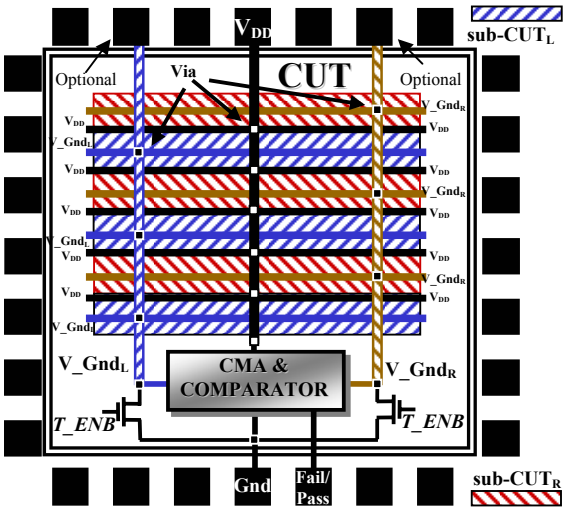

Figure 4: Ground supply rail partition

The proposed PCMA circuit is shown in Fig. 5. It is based on the Wilson current mirror topology that has been selected due to its high output resistance. In general it consists of n branches at the side of the injection current port (*INJCT*) and m at the side of the bias current port (*BIAS*). The formed current mirrors act as current sinks at the virtual ground of the sub-$CUT_{R/L}$ under test in order to bias its background current $I_{B(R/L)}$. Each branch is activated by a distinct select signal SEL_i that drives two switches: a single nMOS and a full CMOS. These select signals provide the programmability of the current mirror. Each combination of activated branches is characterized by a unique amplification factor that gives the ability to synthesize the proper bias current for each test vector that is applied to the CUT.

In order to activate the required state of the PCMA an n+m stages scan register (I_{DDQ} Scan Register - ISR) is utilized. The output of each stage drives the switches of a distinct branch. The "activation" vector that is loaded to the ISR determines which branches will be activated according to the "high" bit positions and thus which will be the current gain $\beta_{L/R}$ of the PCMA. The "activation" vector is loaded serially to the ISR through a scan-in port, for example utilizing the IEEE 1149.1 boundary

scan or the IEEE P1500 embedded core testing standards.

3. Demonstrator and Experiments

3.1 The Demonstration circuit

In order to validate the proposed I_{DDQ} testing technique a demonstration circuit has been designed and fabricated in the standard 0.18μm CMOS technology of ST-Microelectronics (V_{DD}=1.8V). The demonstrator consists of a digital circuit, the PCMA circuit and a comparator that is used to discriminate defect free from defective gates. For each subcircuit all its NAND gates are driven by a pair of signals and all its NOR gates are driven by another pair of signals. These eight signals are exploited to control the background current of the circuit. This current ranges from about 100nA up to 10uA for all input combinations (256 combinations) in all process corners. Obviously, this is a demonstration circuit without any logic implemented on it.

Although the size of the digital circuit is small to provide large background currents, this magnitude is not important in the validation of the proposed technique. What is essential is the ability of this method to discriminate defect free from defective circuits when the background currents and the defective currents (that are

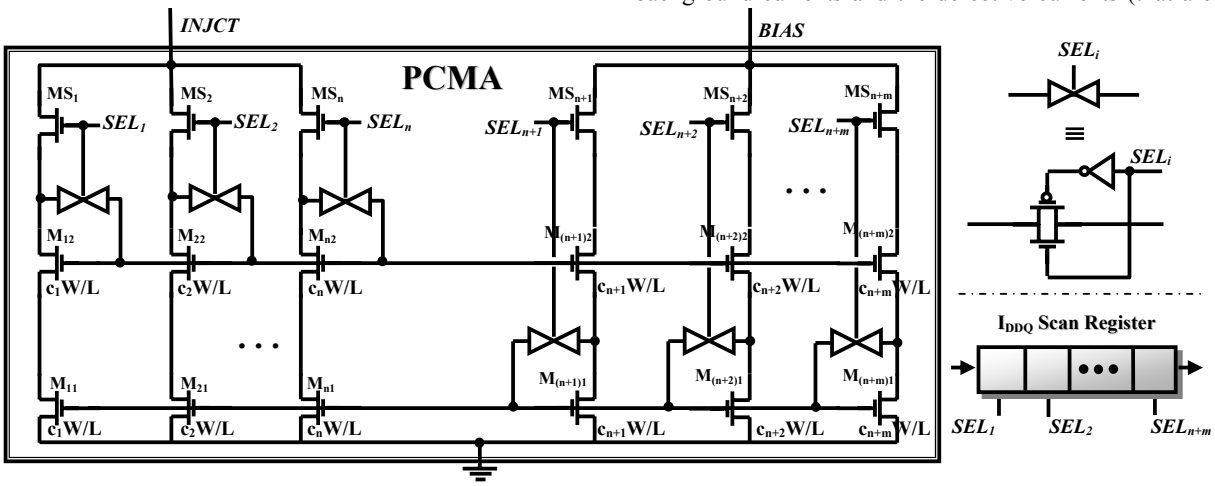

Figure 5: The proposed PCMA circuit

cases. In addition a faulty cell constructed of two inverters with a 1KΩ resistance short circuit between their outputs is present. The faulty cell shares the same virtual ground (V_Gnd) with one subcircuit and can be properly activated by a *Fault_Enable* signal in order to insert a bridging fault in the circuit under test. Furthermore, it is possible to connect externally any desired resistance value between V_{DD} and a V_Gnd node. The microphotograph of the demonstrator is shown in Fig. 6.

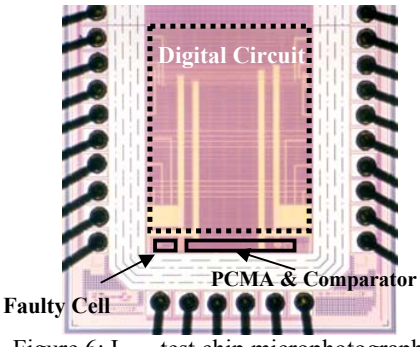

Figure 6: I_{DDQ} test chip microphotograph

A. The digital circuit: This is the CUT and is constructed of 10800 two input NAND and 10800 two input NOR gates, with a total of 86400 transistors. The circuit is partitioned into two subcircuits according to the ground supply partitioning technique of Fig 4. Each subcircuit contains half of the total NAND and NOR

desirable to be detectable) are comparable and a single voltage reference is used for discrimination.

B. The PCMA circuit: It consists of six branches (n=3 and m=3) and thus six select signals are used for programming. The transistor widths for the PCMA branches are: i) first branch W=20μm, ii) second branch W=30μm, iii) third branch W=100μm, iv) fourth branch W=50μm, v) fifth branch W=100μm and vi) sixth branch W=200μm. In all cases the transistor length L is 0.5μm. According to the simulations in all possible process corners, it results that in order to perform I_{DDQ} testing on the CUT, considering all input combinations as test vectors, only 10 states from the total 49 PCMA states are enough.

C. The Comparator: The comparator is a simple differential amplifier. Its main characteristic is the high input resistance useful to avoid the disturbance of the bias mechanism established by the PCMA. One of the comparator's inputs is connected to the *BIAS* port of the PCMA and the other to a reference voltage V_{REF}=0.9V. The comparator has been designed so that its digital output *Fail/Pass* (fault indication signal) provides, during I_{DDQ} testing, a "high" response in case that a fault is present and a "low" response in the fault free case.

The required silicon area for the PCMA and the comparator is only the 2.42% of the CUT. Note that, it is not necessary for the proposed technique either the PCMA or the comparator to be embedded on the chip. External circuits may provide a higher flexibility. The only requirement is the proper partitioning of the CUT.

3.2 Experimental Results

According to the proposed I_{DDQ} testing approach, for every subcircuit and for every input combination (test vector) of the digital circuit a specific activation vector <SEL_1-SEL_6> for the select signals has been determined through simulations in every process corner. This set of activation vectors has been used during the evaluation of the fabricated I_{DDQ} test chip (see Table I). The evaluation procedure was as follows:

a) Initially *T_ENB* is set to "high" and the input vector is applied to the CUT along with the corresponding activation vector. The PCMA and the faulty cell are inactive (fault free case – PCMA inactive).
b) Then the *T_ENB* is set to "low" and the I_{DDQ} test result is observed at the *Fail/Pass* port.
c) The *T_ENB* is set to "high" and the PCMA is activated (fault free case – PCMA active).
d) Next the *T_ENB* is turned to "low" and the *Fail/Pass* signal is read.
e) The *T_ENB* is turned to "high" and the faulty cell is activated (faulty case – PCMA active).
f) Finally, the *T_ENB* is set to "low" for another read of the *Fail/Pass* signal.

This procedure has been followed for every possible input vector and the experimental results have shown that there is never an erroneous fault indication in the fault free case when the PCMA is active and that there is always a fault detection indication when a fault is present and the PCMA is active. This means that the proposed technique fulfills I_{DDQ} testing requirements without any loss either in the yield or the fault coverage. However, as it is illustrated in the logic analyzer view of Fig. 7 there were fault free cases, with the PCMA inactive, where the result was an erroneous fault indication, which means that without the proposed technique these cases will lead to yield loss.

Table I - Test vector distribution per activation vector

Activation Vector <SEL_1-SEL_6>	PCMA Current Gain (β)	Number of Test Vectors
<100 010>	200/20	2
<100 110>	300/20	6
<010 100>	100/30	10
<010 010>	200/30	46
<010 110>	300/30	2
<001 001>	50/100	24
<001 100>	100/100	129
<001 101>	150/100	1
<001 010>	200/100	32
<001 110>	300/100	4
Total Test Vectors:		256

The above procedure has been followed for the internal resistance of the faulty cell as well as for external short circuit resistance values up to 3MΩ (I_{DEF}=600nA) with the same as previous correct behavior. This resolution is determined by the comparator. Note that the range of measured background currents in the fabricated chip was from 400nA up to 2.6μA. Thus, the effectiveness of the proposed I_{DDQ} testing technique to discriminate defect free from defective circuits when the background and the defective currents are of the same magnitude is validated. However, without the proposed technique and considering the expected maximum background current according to the simulations (I_{Bmax}=10μA), the higher detectable defective resistance, using a single I_{INJ} and V_{REF}, without yield loss, would be less than 180KΩ.

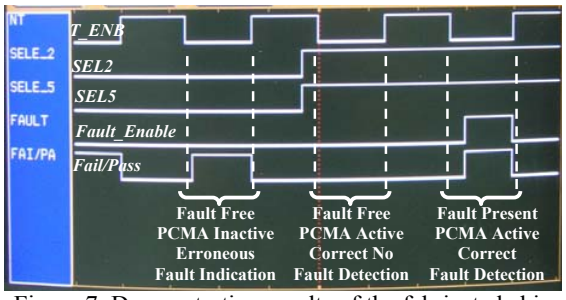

Figure 7: Demonstration results of the fabricated chip

4. Conclusions

In this work a new built-in I_{DDQ} testing circuit and technique are presented. The proposed scheme is capable to overcome problems of I_{DDQ} testing related to technology evolution and provide immunity from possible process and temperature variations as well as the dependence on the applied test vector. The circuit utilizes a single reference voltage to discriminate defect free from defective circuits with high defective current resolutions. Experimental results validate the ability of this scheme to provide high fault coverage without yield loss. The adoption of the proposed technique is a promising solution to extend the viability of I_{DDQ} testing in future technologies.

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