A BIST Scheme for Testing and Repair of Multi-Mode Power Switches*

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***Abstract*—It was shown recently that signature analysis can be used for the test, diagnosis and repair of a robust multi-mode power-gating architecture. A drawback of this approach is that it requires a tester in a production-test environment, and potentially expensive manufacturing steps are necessary to repair defective power switches. We propose a built-in self-test (BIST) and built-in-self-repair (BISR) scheme for test and repair of multi-mode power switches. The proposed method reduces test cost and obviates additional manufacturing steps for post-silicon repair. In addition to eliminating the need for an external tester, it offers protection against latent defects that are manifested as errors in the field. In this way, the robust BIST/BISR solution for power switches enhances the reliability of multi-core chips that employ aggressive power management techniques. Simulation results highlight the low hardware overhead and effectiveness of the proposed method for detecting, diagnosing and repairing defects.**

I. Introduction

The reduction in transistor threshold voltages in deep sub-micron technologies has led to an inevitable increase in leakage current and unacceptably high static power consumption [1]. A number of techniques have been proposed to tackle the problem of high static power dissipation. One technique is to use high-V_t cells in paths with large slack [6]. High-V_t cells reduce static power consumption with negligible impact on circuit performance when they are carefully used in high-slack paths. A more aggressive technique is to completely disconnect the power supply from the core when the core enters the idle mode for a relatively long time period. This is achieved by turning off high-V_t power switches that are used to connect the core to the power supply and/or the ground rail [6], [8].

When power switches are completely turned off, the leakage current is suppressed and there is negligible static power consumption. However, when the power switches are turned on again, a considerable amount of time is required for the core to become active. Therefore, despite their benefits in reducing static power, high-V_t power switches can only be exploited during long periods of inactivity. To overcome this limitation, the techniques proposed in [3], [7], [9] provide one intermediate power-off mode, which reduces the wake-up time at the expense of decreased power savings. The method proposed in [10] extends this approach by supporting multiple intermediate power-off modes. However, it suffers from major shortcomings, which render it inapplicable in realistic applications—it is highly sensitive to process variations and it is not easily testable as it consists of analog components. An efficient and robust power-switch architecture was proposed in [2], [12]; it supports multiple intermediate modes and it is suitable for realistic applications and practical workloads.

The use of power switches in practice requires the adoption of thorough test methods to ensure their defect-free operation. Efficient methods for testing power switches have been proposed in [5], [11]. Unfortunately, these methods are not suitable for multi-mode power switches. In [13] a signature analysis method was proposed for testing and diagnosing multi-mode power switches. The simplicity of this approach and low area overhead make it scalable for multicore chip design with multiple power domains [11]. However, this technique is suitable only for manufacturing test because it requires the use of automatic test equipment (ATE) in a production-test environment. In addition, the repair mechanism proposed in [13] requires specialized and potentially expensive manufacturing steps, which increase the manufacturing cost and area overhead of the power-switch design.

In this paper, we propose a BIST/BISR technique for testing and repairing multi-mode power switches. The proposed BIST scheme completely eliminates the need for external ATEs, thus it reduces the complexity and testing time for manufacturing test. Moreover, it can be used to detect defects in the field, which appear after products have been shipped (due to aging phenomena or electromigration effects), and it provides a mechanism to repair faulty power switches in the field. Finally, the proposed BISR scheme reduces manufacturing cost as it eliminates specialized manufacturing steps that are used in [13] for repairing faulty switches before product delivery.

II. Background

The multi-mode power-switch architecture for two intermediate power-off modes is shown in Fig. 1. It consists of three footer transistors M_p, M_0 and M_1 that are connected between the core and the ground rail. Transistor M_p is a large high-V_t transistor used to switch the core into the power-off mode, which plays the role of a main power switch. It is implemented using several small transistors connected in parallel. M_0 and M_1 are very small low-V_t transistors.

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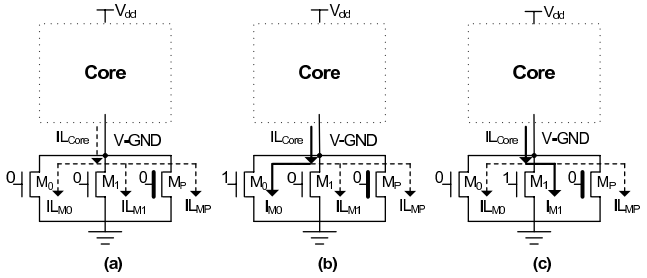

Fig. 1. Power-switch architecture [12].

When M_p is "on", the core operates in the normal functional mode and when it is "off" it disconnects the core from the ground rail. When transistors M_0, M_1 are also turned-off the virtual ground rail ($V-GND$) charges to a voltage level close to the power supply. As a result, the leakage currents of the transistors of the circuit are suppressed and the static power consumption is very low. When M_p is turned on, the core is activated again. However, the aggregate size of the transistors comprising the power switch M_p is relatively small compared to the size of the core and thus it cannot quickly discharge the virtual ground node. Consequently, M_p alone is not sufficient for short periods of inactivity.

In order to tackle this problem, transistors M_0 and M_1 are used to set the virtual ground node to intermediate voltage levels during the power-off mode. Transistor M_0 implements the dream mode and transistor M_1 implements the sleep mode. In the dream mode, transistor M_0 is on and transistors M_p and M_1 are off as it is shown in Fig. 1(b). The difference with the snore mode is that the current flowing through transistor M_0 increases and depending on the size of transistor M_0, it sets the virtual ground node at a voltage level which is lower than that of the snore mode. Consequently, the wake-up time drops but inevitably the static power consumed by the core increases compared to the snore mode.

The sleep mode is implemented by further decreasing the voltage level at the virtual ground node. This is achieved by using transistor M_1, which has larger aspect ratio than M_0 ($W_{M1}/L_{M1} > W_{M0}/L_{M0}$). When M_1 is turned on (M_0 is turned-off), the aggregate current flowing through M_0, M_1, and M_p increases even more and the voltage level at the virtual ground node is further reduced compared to the dream mode (see Fig. 1(c)). As a result the wake-up time decreases at the expense of increased static power consumption, which however remains much lower than the static power of the active mode. Besides M_0 and M_1, additional transistors can be used to offer more power-off modes if they are properly sized, as shown in [2], [12] .

Fig. 2 presents the basic structure proposed in [13] to test the multi-mode power switches. A voltage control oscillator (VCO) consisting of current-starved inverters, with $V-GND$ as control signal, converts the voltage at $V-GND$ into a signal toggling with a frequency that depends on this voltage. The VCO output is connected to the $V-GND$ node and at the same time an intermediate power-off mode is applied. The VCO output triggers a binary counter that provides a quantification of the frequency

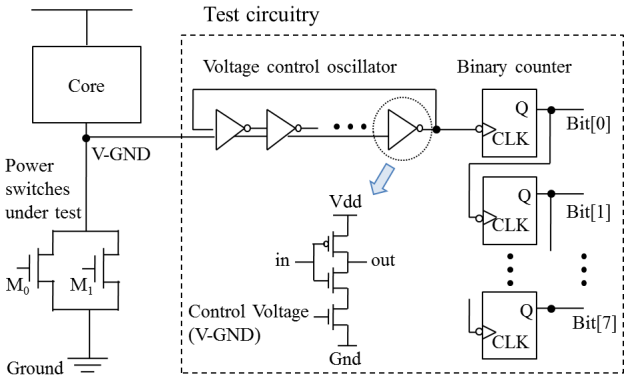

Fig. 2. VCO and VCO counter [13].

as a digital value, which is stored in the counter at the end of the testing period. This value is directly proportional to the voltage at $V-GND$ and it is the signature of the die at the respective power-off mode. The key idea of this test method is to measure the voltage of the virtual-ground node; this approach is generic and applicable to any switch-based power saving architecture.

As shown in [13], the power switches are defect-free if the voltage at $V-GND$ lies between an upper bound and a lower bound. These bounds are refereed to as Test-AARs (Test Adjusted Acceptable Ranges) and they are different for each power-off mode. They correspond to digital signature values which are calculated using simulation. However, excess process variations affect the operation of VCO and shift the signature out of the nominal range of acceptable signature values even when the power switches are defect-free. In order to reduce the effects of process variations, a calibration strategy was adopted in [13] to adjust the die signatures. However, this strategy requires extensive interaction with the tester, which increases both testing time and test cost.

In [13], a repair mechanism was also proposed, which inserts redundancy to replace any faulty power switch with spare fault-free switches. This is a realistic goal as the transistors are small—therefore spare transistors can be introduced at negligible cost. The selection of the non-defective transistors can be done post-manufacture using programmable structures such as laser-cut or electrically programmable fuses (e-fuses) commonly used for memory built-in self-repair. However, laser-cut fuses are characterized by high silicon area requirements ($200\mu m^2$ per fuse is reported in [4]) and they are not scalable with process improvements (they do not scale below the wavelength of the laser beam). In addition, they require a separate and time-consuming manufacturing flow, and this repair solution is not applicable after chip packaging. On the other hand, e-fuses require a higher-than-nominal voltage for their programming, which must be either provided through an additional pad or generated by an embedded voltage generator (charge pump); both these solutions lead to substantial increase in chip cost.

In the remainder of this paper, we present an embedded BIST/BISR scheme that simplifies testing process and facilitates post-silicon repair of defective switches without the need for

fuses or expensive repair steps during manufacturing.

III. Proposed Scheme

A. Testing of Power Switches

Let us assume that die i is tested. Before any power switch is tested, the effects of process variations on the die must be quantified. To this end, instead of the virtual ground node, the power supply voltage is used to drive the VCO for a predetermined number (TL) of clock cycles. During this period the VCO-counter provides a reference signature of die i. This reference signature can be compared to a golden reference signature that is computed in simulation without process variations. The difference D_i between the reference signature of die i and the golden reference signature is the length of the shift, which is caused by the effects of process variations on the VCO.

At the first step the proposed scheme calculates D_i. To this end the VCO counter is initialized to the golden reference value, which can be computed via simulation, is the same for all dies and therefore can be hardwired on chip. The VCO input is connected to V_{dd} and the VCO unit triggers the VCO counter for a period equal to TL clock cycles (defined above). During this period, the VCO counter counts down and it is triggered by the VCO a number of times that is equal to the reference value for the die. At the end of this counting period the VCO counter holds the value D_i.

In order to eliminate the effects of process variations, the proposed scheme measures the signature for each power-off mode for die i and it adjusts this signature by adding to it value D_i (this causes an opposite shift for each signature). The adjusted signature can then be directly compared to the Test-AARs as shown in [13]. Specifically, at the second step, the VCO input is connected to the virtual ground node and the power switch under test is turned-on to put the core into the respective power-off mode (power switch M_p is turned off). The VCO counter is again triggered by the VCO unit and it begins to count up now starting from its current value (i.e., D_i) for a period equal to TL clock cycles as before. During this period the VCO counter will be triggered a number of times equal to the signature value at this power-off mode. When this counting period ends, the VCO-counter value is equal to the adjusted signature of the power switch, i.e., the signature at this mode increased (i.e., shifted) by D_i.

At the third step, the adjusted signature is compared to the lower bound (LB) of the Test-AAR. For this purpose, the VCO counter is disconnected from the VCO output and it is triggered by the system clock for the rest of the testing process. The VCO counter (which contains the adjusted signature value) counts down for a number of cycles equal to the lower bound of the Test-AAR (i.e., it is triggered LB times by the system clock). Then, the value of VCO counter is the difference between the adjusted signature and the lower bound of the Test-AAR. If during this time the VCO counter reached the value 0 then we infer that the adjusted signature was lower than LB. Hence the power switch is defective.

If the lower bound was not violated, the VCO counter continuous to count down again at the fourth step for another $UB-LB$ clock cycles. Note that similar to the golden reference value, UB and LB are known during the design phase; thus they can be embedded on-chip the same way as the golden reference value. At the end of the counting period, the value stored in the VCO counter is equal to the difference between the adjusted signature and the UB. If during this period, the VCO counter reached zero at any point, we infer that the signature is smaller than UB, thus the power switch is defect-free; else the upper bound is violated and the power switch has to be replaced with a spare one. The following example illustrates the operation of the test method.

TABLE I
VCO-Counter Contents for a Test Case Example.

Die	Initial	Step 1	Step 2	Step 3	Step 4	LB	UB
A	202	4	174	10	-6 (250)	Pass	Pass
B	202	4	159	-5 (251)	–	Fail	Pass
C	202	4	184	20	4	Pass	Fail

Example 1. Let us assume that the golden reference value for a design is 202 and that the Test-AAR for a particular power-off mode is [164, 180] (i.e., LB =164 and UB =180). We consider three different dies A, B and C, which are all affected by the same amount of process variations and they all provide the same reference value 198 (in that case $D_A = D_B = D_C = 202 - 198 = 4$). Let the three dies provide the following signatures when the 8-bit VCO counter is triggered by the VCO unit for a period equal to TL clock cycles at the power-off mode (the VCO unit is driven by the virtual ground node during this period): 170 for die A, 155 for die B and 180 for die C. Note that according to [13] the adjusted signatures of these dies are $170 + 4$, $155 + 4$, and $180 + 4$, which imply that A is defect-free (in the range [164, 180]), and dies B, C are defective because their adjusted signatures violate the lower bound and the upper bound of Test-AAR, respectively. For each die, the results of the test process are shown in Table I. Each row presents the results of a die and each column the contents of the VCO counter after each step (the parenthesis show the actual counter value in case of negative results). It is obvious that the proposed scheme correctly identifies the defective dies in all cases. □

B. BIST Architecture

In this subsection, we present the BIST unit that is used for the self-test of one multi-mode power switch at a time. The block diagram is shown in Fig. 3 (we assume here that multi-mode power switch M_j is being tested). The proposed circuit requires the trigger signal TEST_Go to start testing power switch M_j as well as the signal Mode_ID, which indicates the power-off mode that corresponds to M_j. It generates the signal Test_end to indicate when the test ends as well as the signal Pass/Fail to indicate whether the switch under test is good or not. When the power switch fails the test, signals LP_violation, LP_difference and UB_violation are also generated to provide the exact cause of the failure. LB_violation is asserted when the signature violates the lower bound and LB_difference is equal to the difference of the signature from the lower bound. UB_violation is asserted when the signature violates the upper bound.

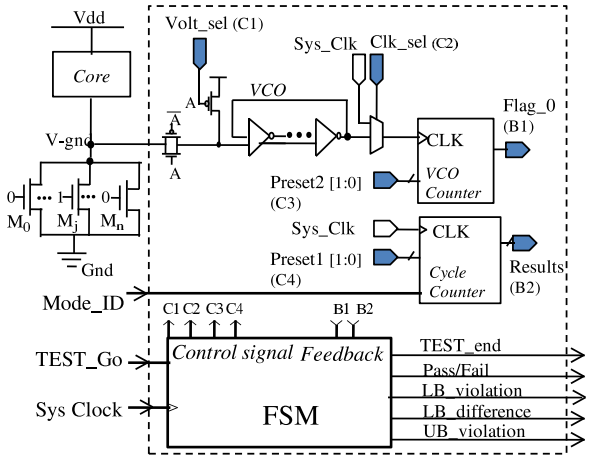

Fig. 3. BIST unit.

TABLE II
OPERATION OF VCO AND CYCLE COUNTERS.

Preset1	VCO Counter	Preset2	Cycle Counter
00	Load Golden Sign.	00	Count Down
01	Count Up	01	Load value TL
10	Count Down	10	Load value LB
11	Hold Value	11	Load value $UB - LB$

The BIST circuitry consists of four main modules: VCO, VCO Counter, Cycle Counter, and FSM (finite state machine). The operations of VCO and VCO counter are similar to the operation of the respective units in [13] with some additional functionalities. The Cycle Counter is used to control the test periods that VCO counter counts up or down. The FSM is used to synchronize the operation of all units during BIST and to carry out the test operations for each power switch.

Four control signals are generated by the FSM: Volt_sel, Clk_sel, Preset1, and Preset2. Signal Volt_sel is used to select the control voltage of VCO. When Volt_sel is high, the input of VCO is connected to the virtual ground node; otherwise it is connected to V_{dd}. Note that in the normal mode of operation the Volt_sel signal remains high to disable the VCO and eliminate its dynamic power consumption. The Clk_sel signal selects the clock source for the VCO counter. When it is high, the output of the VCO output is used as the source of the VCO counter clock, otherwise the system clock is used as the source (in the normal mode of operation the Clk_sel signal remains high to disable the VCO counter). Preset1 is a 2-bit signal and it controls the operation of Cycle Counter. Preset2 is also a 2-bit signal, which controls the operation of the VCO Counter. The corresponding operations of Cycle Counter and VCO Counter are listed in Table II. Note that the values LB and $UB-LB$ loaded into the Cycle Counter are selected based on the value of Mode_ID, which indicates the current power-off mode under test. Whenever the VCO counter reaches value 0, the signal Flag_0 is asserted. Both the final count value of Cycle Counter and the signal Flag_0 from the output of VCO Counter are fed back to the FSM to evaluate the test results.

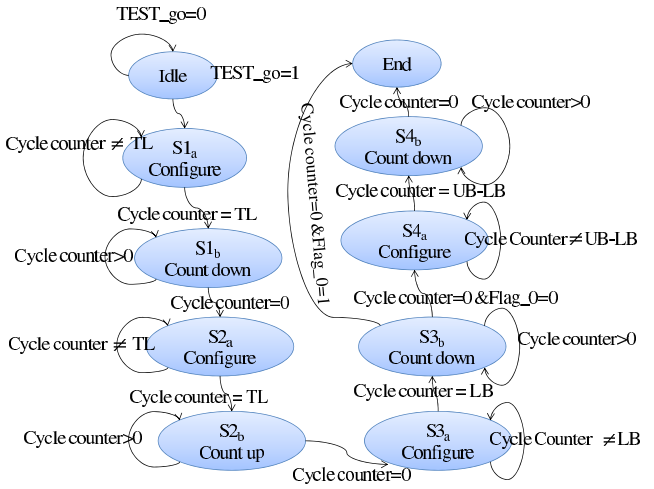

Fig. 4. Finite-state machine for BIST scheme.

The state transition diagram of the FSM is illustrated in Fig. 4. Note that there are two types of states: configuration states and counting states. Configuration states ($S1_a, S2_a, S3_a, S4_a$) are used to configure various parts of the BIST structure while counting states ($S1_b, S2_b, S3_b, S4_b$) are used to enable the counting of the VCO counter. State pairs ($S1_a, S1_b$), ($S2_a, S2_b$), ($S3_a, S3_b$) and ($S4_a, S4_b$) correspond to steps 1, 2, 3 and 4, respectively.

C. BISR Architecture

As shown in [13], the low-cost implementation of the power switch architecture permits the utilization of redundant power switches to replace defective ones. Besides duplicating the multi-mode power switches, additional redundant power switches are also used with their aspect ratios shifted above and below the nominal values to compensate for parametric faults and process variation effects. The BIST unit described in the previous subsection is used to test each power switch. An additional module, the BISR unit, is embedded to co-ordinate the BIST session and to select one power switch for each power-off mode after the test is completed.

The complete BIST/BISR scheme is shown in Fig. 5. When the BIST_Go signal is asserted, the BISR unit selects the first power-off mode and it sets the Mode_ID signal accordingly. Then, it selects one of the power switches corresponding to this mode, it turns this switch on to put the core into the respective power-off mode, and it tests this power switch by asserting the TEST_Go signal of the BIST unit (note that the BIST_Go signal is used to turn-off the main power switch M_p during the whole testing period). When the test finishes (the signal TEST_end is asserted) the status of the signal Pass/Fail is checked to verify whether the power switch passed the test. If the power switch passed the test, it is selected as the power switch of the respective power-off mode and the rest of the power switches for the same power-off mode are not further exercised.

The selection of the power switch is done by appropriately setting the contents of a selection register based on the result of the test. This register drives the input of a decoder that selects one

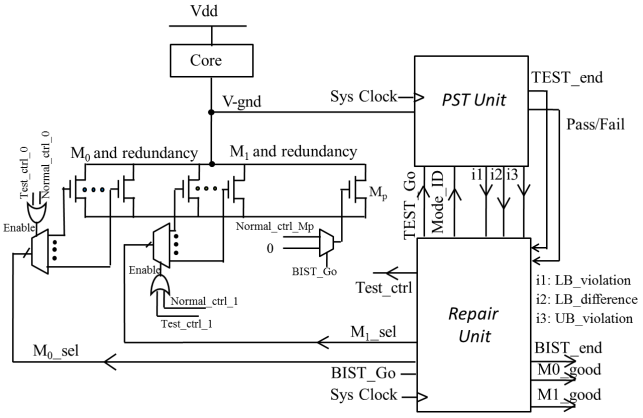

Fig. 5. The complete BIST scheme with built-in self-repair.

of the power switches used for this power-off mode as shown in Fig. 5. Note that the enable input of each decoder is controlled by both the test circuit and the power control unit of the multi-core chip in order to activate/de-activate the power-off mode during both normal operation and test mode. If the power switch failed the test then the next available switch for the current power-off mode is selected and it is tested. When all power switches corresponding to a power-off mode are tested, the BISR unit continues with the next batch of power switches for the next power-off mode.

There might be cases when none of the power switch complies with the signature specifications. In these cases, we can still select a power switch that violates the lower bound. As shown in [13], when the signature violates the lower bound of the Test-AAR, then the only effect is an increase in the static power dissipation of this mode (the wake-up time drops) and the power switch is still functional. Among the power switches failing the lower bound, the one with the signature that deviates the least from the lower bound is selected because it offers the highest reduction of static power in the power-off mode. Signal LB_difference transfers the difference between the signature and the lower bound to the BISR module. When signal LB_violation is asserted, the value of LB_difference signal is transferred to an internal register. If the register already holds a value from a previously selected power switch (which was also found to violate the lower bound) then it is updated with the new value only if this is smaller than the previous one. At the same time, the selection signals of the power switches are also updated to select the new transistor.

The flow diagram of the BISR operation is shown in Fig. 6. The proposed scheme receives a trigger signal (BIST_Go) from an external unit (e.g. a processor) whenever the testing has to be performed. Subsequently it begins to test the power switches starting from the M_0 switches. It selects one M_0 switch at a time until it finds a non-defective one. Then it proceeds to the testing of M_1 switches (the next power-off mode) in the same way. When all switches are tested, signal BIST_end is asserted to notify the external unit the end of the testing operation.

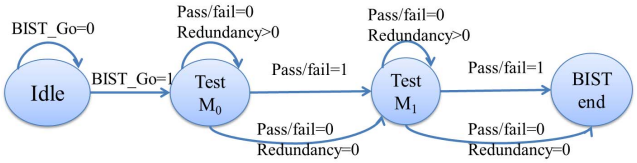

Fig. 6. BIST and Repair State Diagram

IV. Experimental Results

We implemented the proposed scheme and we run several simulations in order to evaluate its effectiveness. We assumed a logic core consisting of nine million transistors which is representative of a realistic industrial circuit in terms of static power consumption during DC operation. We used the 45 nm predictive technology [14] for 1.1 volts power supply. The clock frequency of this core was set to 1 Ghz and the static power consumption of the core in idle mode (without the use of power switches) is equal to 10 mW. We attached to this core a power switch M_p implemented as a number of smaller transistors connected in parallel, with aggregate size equal to 43.2×10^6 nm (this size was selected to be equal to the 12% of the total width of the nMOS transistors in the logic core as suggested in [10]). The length of M_P was set equal to 45 nm. We also attached to the core a number of multi-mode power switches for two intermediate power-off modes: the dream mode and the sleep mode. For each power-off mode we used a triplet of multi-mode power switches M_0, M_1 respectively. According to the design method proposed in [12] the nominal size (W, L) of the M_0 switches is equal to (250 nm, 45 nm) and the nominal size of the M_1 switches is equal to (480 nm, 45 nm). As suggested in [13] we varied the width of the two switches of each tripplet by 10% above and below the nominal values in order to tolerate process variation effects and parametric faults. The VCO unit was implemented using 9 current-starved inverters. The voltage range of interest at the V-GND node is 350 to 800 mV, and for this range the frequency of the VCO was measured using Spice simulations in the range 0.64 GHz to 9.1 GHz.

We implemented the proposed scheme using Verilog. The BIST circuitry was designed at RT level and it was synthesized to gate-level using Synopsys DC compiler. The synthesized gate-level description was then simulated using the Synopsys VCS simulator. The synthesized gate-level design consists of 64 flip-flops and 239 logic gates. In particular, the BIST unit consists of 42 flip-flops and 151 logic gates, and the BISR unit consists of 22 flip-flops and 88 logic gates. The static power of the BIST and BISR, estimated using HSPICE, is approximately 3.8 μW in the non-test mode. TL was set equal to 20 system clock cycles. When the input of the VCO is connected to V_{dd}, and assuming no process variations, the VCO unit triggers the VCO counter 202 times in the period of TL (i.e., 202 is the golden reference value). The values of LB, UB were found to be equal to $LB = 72$, $UB = 80$ for the dream mode and $LB = 23$, $UB = 29$ for the sleep mode.

Table III presents the test results of the BIST unit for a particular test case where random parametric faults have been

TABLE III
A TEST CASE

Power Switch Under Test	LB violation	UB violation	LB difference	adjusted signature
1st M_0	0	1	—	82
2nd M_0	1	0	3	69
3rd M_0	1	0	12	60
1st M_1	0	0	—	26

injected. The first column presents the switches under test in the specific order that they are tested. The next three columns present the test results of BIST unit, and the last column of the table presents the adjusted signature. At first, the BISR unit activates the first M_0 switch, it sets appropriately the status of the signal Mode_ID and it asserts the signal Test_Go to start the testing process. When the signal Test_End is asserted the BISR unit detects that the first M_0 violates the upper bound. Therefore, this switch is discarded as defective and the BISR unit continues to test the second M_0 power switch using the same process. After the testing process for the second M_0 finishes, it is found that this switch violates the lower bound. This means that it can be used, but with reduced power saving benefits. To this end, the BISR unit temporarily selects this switch and also stores the difference of the signature of this switch to the lower bound. Since there is an additional power switch available for this power-off mode (the 3rd M_0 switch) the same process is repeated by the BISR unit. The test outcome for the third M_0 switch indicates that this switch violates the lower bound of the Test-AAR to a larger extent than the temporarily selected power switch. To this end, this power switch is also discarded. At this point, all M_0 power switches have been tested and the BISR unit proceeds to the testing of M_1 power switches. Since the first M_1 is found to be defect-free, it is selected by the BISR unit and the BIST session terminates.

The test time depends on the (intermediate) outcomes of the test procedure. Note that the test process for the switches corresponding to an intermediate power-off mode terminates as soon as a non-defective switch is found. Moreover, when violation of the lower bound is detected the test process of the power switch terminates immediately. Therefore, the testing process for fault-free power switches as well as for power switches violating the upper bound takes a few cycles longer than the testing process for power switches violating the lower bound. The worst case with respect to the testing time occurs only when all power switches of a power-off mode violate the upper bound or when only the last tested switch is non-defective and the rest ones violate the upper bound.

Table IV presents the test times required for testing the power switches of the implemented circuit. The testing time of the above test-case is 435 clock cycles. In particular, the testing time of the first M_0 power switch is 126 clock cycles. The testing times of the second M_0 and the third M_0 are 117 clock cycles for each one of them. Finally, the testing time of the first M_1 is 75 clock cycles. Assuming that a system clock frequency is equal to 1 GHz, the testing time of the above test case is 435 ns,

TABLE IV
TEST TIMES FOR POWER SWITCHES FOR VARIOUS SCENARIOS.

switch under test	LB violation	UB violation or fault-free
M_0	117 clock cycles	126 clock cycles
M_1	68 clock cycles	75 clock cycles

and the testing time of the best (worst) case scenario is equal to 201 ns (585 ns).

V. CONCLUSIONS

We have presented a BIST/BISR scheme for test and repair of multi-mode power switches. The proposed scheme requires negligible area overhead and short test application time, hence BIST and BISR can be carried out at low cost. Moreover, it offers complete protection against manufacturing defects as well as latent defects affecting multi-mode power switches. While the BIST/BISR hardware is also subject to defects, and process variations, it occupies only a negligible part of the die area, and it can be tested using an ATE before the product is shipped. Thus the proposed scheme can be effectively used to enhance the reliability of multi-core chips that employ aggressive power management techniques.

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