Test Response Compaction by an Accumulator Behaving as a Multiple Input Non-Linear Feedback Shift Register

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Abstract

In this paper we show that an accumulator can be modified to behave as a Non-Linear Feedback Shift Register suitable for test response compaction. The hardware required for this modification is less than that required to modify a register to a Multiple Input Linear Feedback Shift Register, MISR. We show with experiments on ISCAS'85, ISCAS'89 benchmark circuits and various types of multipliers that the post-compaction fault coverage obtained by the proposed scheme is higher than that of the already known accumulator based compaction schemes and in most cases identical to that achieved using a MISR.

1. Introduction

Today's complex electronic products are harder to test using traditional external methods. *Built-In Self-Test (BIST)* can frequently be used without significantly increasing a product's size, cost and production time [1].

BIST structures usually consist of two distinct components [2]: (a) a *Test Pattern Generator (TPG)* which produces and applies test vectors to a *Circuit Under Test (CUT)* and (b) a *Response Analyzer* which collects output responses from the CUT and compares them with the fault-free responses. Since the number of test vectors applied to a CUT is usually large, storing the fault-free response for every test vector on-chip would result to a large area overhead. *Response Compaction* techniques are used therefore to compact the output responses to a short pattern that is called a *signature*. Response Analysis is then limited to comparing the signature that is produced after applying the test vectors with the fault-free signature.

The problem with response compaction techniques is that there is a possibility that a faulty and a fault-free circuit might have the same signature although the CUT's output responses are different. This is called *aliasing*. Every response compaction scheme must achieve three goals: (a) it has to be easy to implement (introduce small area overhead), (b) the signature must be relatively small and (c) the probability of aliasing has to be as small as possible.

An efficient test-response compaction scheme is essential for any reliable BIST. The most commonly used compactors for compaction of parallel responses are based on *Multiple Input Linear Feedback Shift Registers (MISRs)* [2]. General-purpose systems based on a data-path architecture, as well as digital signal processing circuits, or even digital filters, contain either accumulators composed of binary adders and registers, or arithmetic logic units that can perform binary addition. The availability of accumulators in a wide range of circuits justifies the investigation of their suitability for compacting functions. If they could be used to compact test responses, then the need for extra hardware could be drastically reduced.

Hence, several accumulator-based compaction schemes [3-6] were proposed and their efficiency was considered. A response compaction scheme using a counter and an accumulator was proposed in [3]. In the second scheme, called *Accumulator-Based Compaction (ABC)* [4], the accumulator consists of an adder, 2's or 1's complement, and a register for compacting the output responses. In the third scheme, the carry output of the adder is fed back to the adder and is added with the next response of the CUT. This scheme is called *Rotate Carry Adder (RCA)* [5]. The quality of the above schemes was further examined in [7-8]. Recently, another accumulator-based compaction scheme, the *Cascaded Compaction scheme (CC)*, was presented in [6]. This scheme is based on the use of two accumulators. The first one consists of a 2's complement adder and a register while the second one consists of a 1's complement adder and a register. The authors of [6] shown that the aliasing probability of this scheme is significantly less than that in the other accumulator-based compaction schemes. The fact that two adders are required as well as the fact that the first one must be 2's complement while the other 1's complement, restrict the types of circuits that two such adders exist. In all other circuits the hardware overhead due to the addition of a second accumulator is large. Two other accumulator-based compaction schemes for some special circuits have also been proposed in [9-10]

It has been shown [8] that in accumulator-based response compaction schemes the probability of aliasing approaches its limiting value not as fast as in MISRs. The necessary use of more types of gates than XOR, for the implementation of an adder, makes difficult the modification of an accumulator to behave, in test mode, as

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a MISR. The author of [11], based on experimental results, asserts that test response compaction using a non-linear feedback shift register offers higher post-compaction fault coverage than MISRs. Taking into account the above, in this paper we show that an accumulator can be modified to behave as a non-linear feedback shift register, suitable for test response compaction. Given that an accumulator exists, the hardware overhead for the implementation of the proposed scheme is significantly smaller than that required for the implementation of the Cascaded Compaction scheme as well as for the implementation of a MISR. The post-compaction fault coverage obtained by the proposed scheme is higher than that of the already known accumulator-based compaction schemes and in most cases identical to that achieved using a MISR.

The paper is organized as follows. Section 2 refers to the evaluation of the already known accumulator-based compaction schemes. In Section 3 we present the new accumulator-based compaction scheme. In Section 4 we present experimental results on ISCAS'85 benchmarks, ISCAS'89 benchmarks and various types of multiplier circuits that show the superiority of the proposed scheme.

2. On the evaluation of accumulator-based response compaction schemes

We consider an accumulator for *k*-bit operands and that at the first step of the test session the register of the accumulator is initialized to zero. We denote the content of the register after the application of the t-th test vector as R_t, and the output response from the CUT as O_t.

According to ABC [4] (see Figure 1), the output response of the CUT is added to the previous contents of the register and the sum is stored back to the register. The content of the register is given by the following formula:

$R_t = (O_t + R_{t-1}) \bmod 2^k$, for 2's complement adder, and
$R_t = (O_t + R_{t-1} + C_t) \bmod 2^k$, for 1's complement adder,

where C_t denotes the carry-out, C_{out}, output of the adder that is fed back to the carry-in input, C_{in}.

After applying all test vectors, the final content of the register is compared to the fault-free signature for deciding whether the circuit under test is faulty or not. In the cases that the circuit already has an adder and a register, ABC does not impose any additional hardware overhead. The aliasing in the ABC scheme with 2's complement adder can be attributed to two reasons: (a) *error cancellation*, where errors produced by one test vector can be masked by the errors produced by another test vector and (b) *error leakage*, because of an overflow in the adder. The probability of aliasing for the case of 2's complement adder is equal to $1/2^{k-i}$, where i is the number of the least significant bits that are not affected by the fault. This means that the probability of aliasing is high for all those faults that affect only the most significant bits of the outputs. In the ABC scheme with 1's complement adder the aliasing stems exclusively from error cancellation. The probability of aliasing in this case tends to $1/(2^k-1)$ for the class of primitive faults [4, 8]. For long test sequences the aliasing probability of the ABC scheme with 1's complement adder approaches the aliasing probability of MISRs.

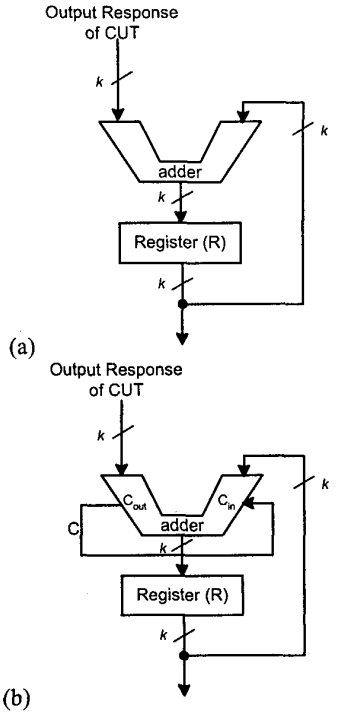

Figure 1: ABC for response compaction: (a) with 2's complement adder, (b) with 1's complement adder

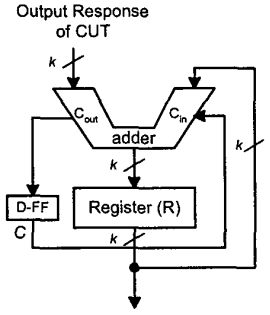

Figure 2: RCA for response compaction

The above analysis implies that the aliasing probability is smaller in the case that the ABC scheme uses a 1's complement adder. However in general purpose systems, and many other cases, 2's complement arithmetic is used. In these cases a 2's complement adder exists. Then to achieve small probability of aliasing, as in the case of 1's complement adders, a new accumulator-based response compaction scheme was proposed [5]. This scheme is

called Rotate Carry Adder, RCA, and is presented in Figure 2. In this scheme the carry out of the adder is stored into a flip-flop and is added to the contents of the register together with the next output response of the CUT. The content of the register is given by the following formula:

$$R_t = (O_t + R_{t-1} + C_{t-1}) \bmod 2^k$$

In the RCA scheme the error leakage is minimized since only the carry-out of the last addition is ignored. Assuming that an adder and a register are already parts of the design, RCA requires only one D flip-flop and therefore the hardware overhead is negligible. The RCA scheme implements the same function as the ABC with the 1's complement adder. Their only difference is that RCA adds the carry output bit with the next output response whereas the ABC adds the carry output bit with the current output response. The probability of aliasing using RCA tends also to $1/(2^k-1)$ for the class of primitive faults [5, 8] and for long sequences approaches the aliasing probability of MISRs.

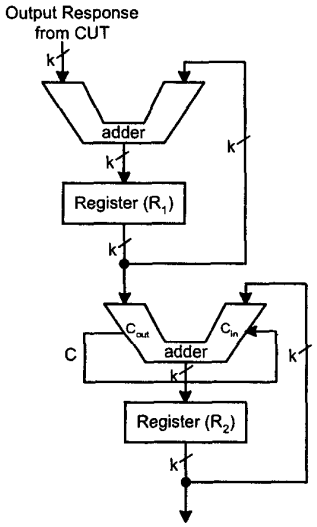

Figure 3: CC for response compaction

In order to reduce the error cancellation, the use of two accumulators has been presented in [6] (see Figure 3). This scheme is called CC. The first accumulator performs 2's complement addition whereas the second accumulator performs 1's complement addition. The content of the two registers are given by the following formula:

$$R_{1,t} = (O_t + R_{1,t-1}) \bmod 2^k$$
$$R_{2,t} = (R_{1,t-1} + R_{2,t-1} + C_t) \bmod 2^k$$

Although this scheme has small probability of aliasing, it imposes large hardware overhead. Since two accumulators are required and the first must realize 2's complement addition while the other 1's complement addition, the class of circuits that include two such accumulators is restricted. For the circuits that only one of the required adders is already part of the design, CC requires an extra adder for its implementation.

3. The proposed response compaction scheme

This section consists of two subsections. In the first one we propose the new response compaction scheme capable of reducing significantly both error leakage and error cancellation. We also show that this scheme, in fact, turns the accumulator into a non-linear feedback shift register. In the second part we discuss the overhead of the proposed scheme.

3.1 Description of the proposed scheme

We consider an accumulator for k-bit operands. We denote the content of the register after the application of the t-th test vector as $R_t = (r_{t,k}, r_{t,k-1}, \ldots, r_{t,1})$, the output response from the CUT as $O_t = (o_{t,k}, o_{t,k-1}, \ldots, o_{t,1})$ and the value of a D flip-flop as X_t. At the first step of the test session the register of the accumulator and D flip-flop is initialized to zero. Our scheme realizes the following addition:

		$o_{t,k}$	$o_{t,k-1}$	...	$o_{t,2}$	$o_{t,1}$
+	$r_{t-1,k}$	$r_{t-1,k-1}$	...	$r_{t-1,2}$	$r_{t-1,1}$	X_{t-1}
	X_t	$r_{t,k}$	$r_{t,k-1}$	...	$r_{t,2}$	$r_{t,1}$

Based on the above, we conclude that the content of the accumulator's register is given by the formula:

$$R_t = (O_t + (2R_{t-1}) \bmod 2^k + X_{t-1}) \bmod 2^k$$

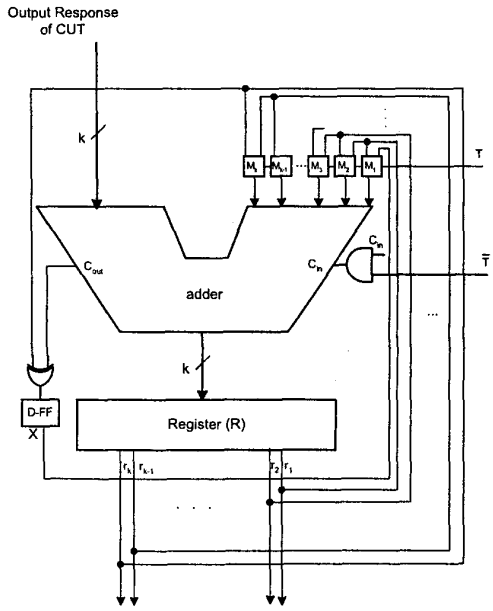

Figure 4: The proposed scheme for response compaction

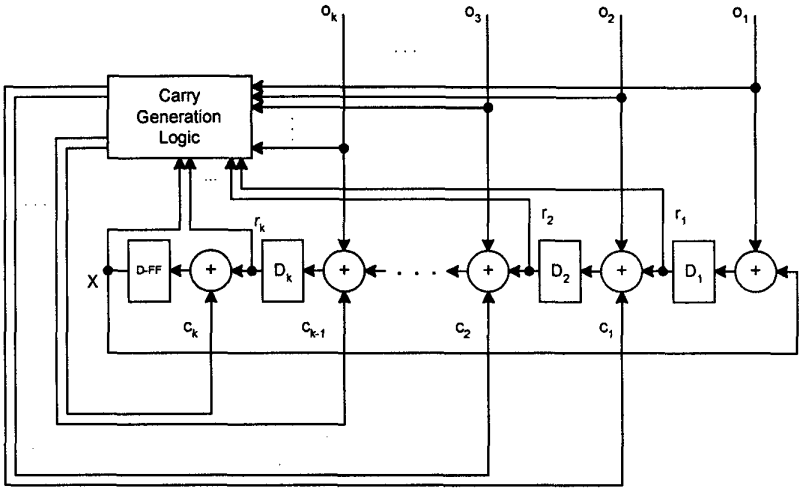

Figure 5: The proposed scheme behaving as a Multiple Input Non-Linear Feedback Shift Register

The proposed response compaction scheme is presented in Figure 4. The contents of the register are shifted one position to the left and then are added with the output response and the value X_{t-1} of the D-FF flip-flop. We store the k-bit of the result back in the register and the $(k+1)$-bit at the D-FF. The shifting operation is implemented by the multiplexers $M_1, M_2, \ldots, M_k$. During test mode the carry-in input of the adder is set to zero.

From Figure 4 we can easily see that, during test mode, T=1, the accumulator behaves as the Non-Linear Feedback Shift Register given in Figure 5. At the end of the test session the register R, in Figure 4, or equivalently the D flip-flops $D_1, D_2, \ldots, D_k$, in Figure 5, contain the signature. Based on the argument of [11] that test response compaction based on non-linear feedback shift register can offer higher post-compaction fault coverage than MISR, we expect that the proposed accumulator-based compaction scheme will give good results. This will be verified in the next section.

3.2 Area and delay overhead of the proposed scheme

At first we will consider the hardware overhead of the proposed scheme. To make our comparisons we use gate equivalents. Using the Synopsys tools driven by the AMS CUB implementation technology (0.6μm, 2-metal layer, 5.0V) and taking one 2-input NAND or one 2-input NOR gate equal to 1 gate equivalent, we get: one 2-input XOR gate equals 2.0 gate equivalents, one 2-input AND gate equals 1.3 gate equivalents, one D flip-flop equals 3.6 gate equivalents and one Full-Adder equals 7.9 gate equivalents. A 2-1 multiplexer equals 1.7 gate equivalents whereas a k-bit adder (for example ripple carry adder) equals $7.9k$ gate equivalents. k is equal to the number of primary outputs of the circuit under test.

If we assume that an adder and a register are already parts of the design, then the hardware overhead for MISR is $3.0k+2.0n$ gate equivalents since we need k NOR gates, k XOR gates and n XOR gates for the feedbacks. The hardware overhead for ABC is 0 while the hardware overhead for the RCA is 3.6 gate equivalents (one D flip-flop). The CC requires one additional register and one additional adder resulting in a hardware overhead of $11.5k$ gate equivalents. The hardware overhead for the proposed scheme is $1.7k+4.9$ gate equivalents.

We can see that the hardware overhead for the cases of ABC and RCA is negligible. However there are cases where these two schemes are not suitable since they introduce considerable aliasing (this will be clearer in the next section). Furthermore there are applications that demand for negligible aliasing. In these applications the designer has to select between a MISR, a CC and the proposed scheme. Comparing these three schemes it is evident that the proposed scheme has the least hardware overhead (assuming that the design already contains an accumulator).

It is evident that multiplexers are not inserted in the critical path of the circuit. Therefore, performance degradation during normal operation of the circuit does not exist.

4. Experimental Results

In order to validate the effectiveness of the proposed scheme, we have performed several simulations. We use a fault simulation program that implements the various response compaction schemes and computes the signatures for every single stuck-at fault in the circuit. Our program doesn't use collapsed fault sets. Instead, it considers

Table 1: Post-compaction fault coverage percentage drop for ISCAS'85 using pseudo-random test sets

	c1355nr	c1908nr	c2670nr	c3540nr	c432nr	c499nr	c5315nr	c6288nr	c7552nr	c880nr
Number of Vectors	1301	4365	550	2075	503	667	1477	31	1058	4111
Pre-Compaction FC	100.00	100.00	83.46	99.74	100.00	100.00	100.00	100.00	95.01	100.00
ABC	2.41	3.77	3.40	2.65	8.95	2.34	1.11	1.01	8.30	4.43
RCA	1.74	0.74	0.54	0.09	1.07	1.83	0.13	0.79	2.63	0.17
CC	0.00	0.05	0.10	0.15	2.39	0.00	0.05	0.13	0.32	0.17
Proposed Scheme	0.00	0.00	0.00	0.00	0.60	0.00	0.00	0.00	0.00	0.00
MISR	0.00	0.00	0.00	0.00	0.60	0.00	0.00	0.00	0.00	0.00

Table 2: Post-compaction fault coverage percentage drop for ISCAS'89 using pseudo-random test sets

	s1196	s1238	s1423	s1488	s1494	s208	s298	s344	s349	s382	s386	s400
Number of Vectors	8692	7437	990	1189	1068	523	85	60	63	99	672	185
Pre-Compaction FC	99.04	95.96	98.10	99.23	98.46	99.31	99.16	99.10	98.68	99.08	99.09	98.50
ABC	1.97	2.62	1.16	5.04	4.48	3.90	4.19	1.94	3.97	3.27	5.70	2.62
RCA	0.00	0.00	0.14	0.00	0.03	1.14	0.50	0.89	0.59	1.57	0.00	0.87
CC	0.00	0.04	0.21	0.10	0.50	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Proposed Scheme	0.00	0.00	0.14	0.00	0.00	0.23	0.00	0.00	0.00	0.00	0.00	0.12
MISR	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

	s420	s444	s510	s526	s5378	s641	s713	s820	s832	s9234	s953
Number of Vectors	10829	114	211	1356	4746	1994	1807	5746	3954	7132	6993
Pre-Compaction FC	90.39	96.62	99.22	98.95	97.86	99.06	94.04	99.02	98.02	85.06	99.00
ABC	2.07	3.83	13.93	2.18	0.16	1.41	0.63	15.67	15.99	0.49	0.63
RCA	0.43	1.46	0.00	0.00	0.13	0.00	0.00	0.00	0.12	0.39	0.00
CC	0.22	0.11	2.06	0.00	0.00	0.00	0.00	0.00	0.12	0.00	0.00
Proposed Scheme	0.22	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MISR	0.32	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

all single stuck-at faults of the circuit. Since the ABC scheme with 1's complement adders gives similar results, with respect to aliasing, with the RCA scheme, in the following Tables results for the ABC scheme with 1's complement adder are not presented.

At first we compare the various response compaction schemes, including the proposed in Section 3, using random test sets generated by LFSRs. For each one of the non-redundant versions of the ISCAS'85 benchmarks, we choose a primitive polynomial and produce a test set with a certain fault coverage before compaction. These benchmarks include a number of typical data-path circuits. We use the algorithm given in [12] to select the seed of the LFSR so as to achieve the target fault coverage with a small number of test vectors. We then measure the fault coverage for each of the response compaction schemes using this test sequence. The results are shown in Table 1. The first row indicates the circuit's name and the second row indicates the number of vectors that are needed to achieve the pre-compaction target fault coverage of the third row. The remaining rows present the post-compaction fault coverage percentage drop for each response compaction scheme.

We can see that: The post-compaction fault coverage drop in ABC is high for these circuits. The use of carry feedback in RCA decreases aliasing and improves the post-compaction fault coverage. CC provides even better results. Aliasing in all circuits, but c3540nr and c432nr is less than that of the RCA.

On the other hand, the use of MISR produces zero aliasing in all circuits except c432nr. These results show the good characteristics of the MISR. The proposed scheme achieves the same results with MISR for these circuits. Although this doesn't prove that the two schemes are equivalent, it strongly suggests that the proposed scheme produces extremely low aliasing and therefore can be used in all circuits that include an accumulator since its implementation cost is smaller than that of a MISR.

We repeat the same experiment using the combinational parts of the ISCAS'89 benchmark circuits.

Table 3: Post-compaction fault coverage percentage drop for ISCAS'85 using compacted test sets

	c1355nr	c1908nr	c2670nr	c3540nr	c432nr	c499nr	c5315nr	c6288nr	c7552nr	c880nr
Number of Vectors	86	117	92	206	52	59	114	27	162	49
Pre-Compaction FC	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00
ABC	8.91	7.17	5.72	3.03	4.89	1.02	1.53	1.36	8.42	6.42
RCA	8.17	4.01	4.72	0.44	1.91	0.31	0.65	0.96	3.78	2.39
CC	0.22	0.21	0.73	0.09	1.31	0.10	0.06	0.23	0.49	0.45
Proposed Scheme	0.00	0.24	0.22	0.00	0.36	0.10	0.00	0.02	0.08	0.34
MISR	0.00	0.00	0.00	0.00	1.07	0.10	0.00	0.00	0.00	0.06

Table 4: Post-compaction fault coverage percentage drop for ISCAS'89 using compacted test sets

	s1196	s1238	s1423	s1488	s1494	s208	s298	s344	s349	s382	s386	s400
Number of Vectors	144	148	58	116	112	35	30	20	21	32	70	35
Pre-Compaction FC	100.00	96.77	99.09	100.00	99.46	100.00	100.00	100.00	99.41	100.00	100.00	98.50
ABC	2.68	2.26	1.02	4.27	3.78	6.65	3.69	4.03	2.50	3.27	4.79	2.75
RCA	0.29	0.08	0.50	0.10	0.16	1.15	0.50	0.00	0.73	2.36	0.52	1.75
CC	0.25	0.12	0.28	0.71	0.63	1.83	1.34	0.45	0.00	0.52	0.52	0.62
Proposed Scheme	0.13	0.00	0.00	0.13	0.10	0.23	0.00	0.00	0.59	0.39	0.13	0.00
MISR	0.00	0.00	0.00	0.10	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

	s420	s444	s510	s526	s5378	s641	s713	s820	s832	s838	s9234	s953
Number of Vectors	71	33	63	62	152	41	40	100	101	144	227	87
Pre-Compaction FC	100.00	97.52	100.00	99.90	98.86	100.00	94.88	100.00	98.98	100.00	93.95	100.00
ABC	4.04	3.49	10.78	2.18	0.45	0.71	1.33	7.62	7.69	3.57	1.87	0.47
RCA	1.31	1.46	0.10	0.47	0.38	0.00	0.00	0.00	0.00	1.71	1.77	0.00
CC	0.00	2.14	1.57	0.66	0.00	0.00	0.49	2.32	1.38	0.05	0.00	0.16
Proposed Scheme	0.11	0.11	0.39	0.00	0.00	0.00	0.21	0.30	0.66	0.00	0.00	0.21
MISR	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.00	0.00	0.00	0.00	0.05

We consider the majority of these benchmarks. We exclude from our experiment the circuits with more than 256 primary inputs or primary outputs because of limitations of our fault simulation program. The results, shown in Table 2, lead to similar conclusions as before.

In Tables 3 and 4 we give simulation results based on compacted test sets derived using Test Synthesis tools by Synopsys. We can easily see that in many cases the proposed scheme has the same post-compaction fault coverage with the MISR scheme while in the rest cases the results are comparable. We have to note that evaluation of a test response compaction scheme can not be based on the use of extremely small test sets. When the test set is very small, the post-compaction fault coverage depends very much on the specific test vectors of the test set. For example in Table 5 we give the post-compaction fault coverage for four different deterministic compacted test sets generated by the Test Synthesis tools by Synopsys for the c499nr benchmark circuit. It is easy to see that depending on the specific test set we can derive different conclusions about the most effective scheme. Results based on compacted test sets are useful only when the test set is embedded in a ROM. Applying any other test set embedding technique, along with the vectors of the test set some extra vectors, not belonging to the test set, are also applied to the CUT. Then, due to the extra vectors, the post-compaction fault coverage gets a new value, which should be derived.

Table 5: Using compacted test sets leads to different evaluation results
(example using c499nr benchmark circuit)

	1st test set	2nd test set	3rd test set	4th test set
Number of Vectors	53	56	60	59
Pre-Compaction FC	100.00	100.00	100.00	100.00
ABC	0.81	0.61	1.02	1.02
RCA	0.00	0.00	0.31	0.31
CC	0.10	0.00	0.61	0.10
Proposed scheme	0.41	0.20	0.00	0.10
MISR	0.41	0.00	0.00	0.10

Table 6: Post-compaction fault coverage percentage drop for multiplier circuits using test sets produced by TPGs

	Carry Save Array Multipliers								
	8x8			16x16			32x32		
	Cell1	Cell2	Cell3	Cell1	Cell2	Cell3	Cell1	Cell2	Cell3
Number of Vectors	192	192	192	192	192	192	192	192	192
Pre-Compaction FC	99.77	99.11	99.43	99.84	99.47	99.61	99.90	99.71	99.78
ABC	5.45	2.34	3.48	1.85	0.35	0.89	1.01	0.08	0.44
RCA	1.47	0.00	0.21	1.05	0.00	0.21	0.81	0.00	0.27
CC	0.91	0.71	0.42	0.06	0.03	0.04	0.03	0.01	0.01
Proposed Scheme	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MISR	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

	Modified Booth Multipliers with Wallace-tree summation								
	8x8			16x16			32x32		
	Cell1	Cell2	Cell3	Cell1	Cell2	Cell3	Cell1	Cell2	Cell3
Number of Vectors	96	96	96	96	96	96	112	112	112
Pre-Compaction FC	99.54	99.60	99.60	99.20	99.35	99.35	99.37	99.51	99.51
ABC	6.27	4.80	5.12	2.74	1.40	1.58	1.54	0.57	0.70
RCA	0.87	0.71	0.71	0.49	0.38	0.40	0.31	0.19	0.22
CC	0.23	0.20	0.20	0.04	0.05	0.02	0.01	0.00	0.00
Proposed Scheme	0.09	0.23	0.08	0.00	0.00	0.00	0.00	0.00	0.00
MISR	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

In Table 6 we give simulation results based on test pattern sequences generated by counter-based TPGs proposed in the open literature for BIST in various types of multipliers [13-14]. We consider two types of multipliers: (a) Carry Save Array Multipliers and (b) Modified Booth multipliers with Wallace Tree summation and full Carry Look-Ahead Adder for the final addition.

For each type of multiplier and for each multiplier size (8x8, 16x16 and 32x32) we use three different gate implementations denoted as Cell1, Cell2 and Cell3.

Results from Table 6 confirm previous results. ABC is inadequate to provide large post-compaction fault coverage especially in circuits with small number of primary outputs (as in the case of 8x8 multiplier circuits). On the other hand, RCA, by the use of carry feedback, decreases error leakage and offers good post-compaction fault coverage especially in larger circuits. In small multiplier circuits though, the post-compaction fault coverage drop is in many cases more than 1%. MISR produces zero aliasing in all cases.

The proposed scheme is similar to MISR and produces zero aliasing in all cases except for 8x8 Wallace multipliers. Even in these cases, the proposed scheme performs better than the other accumulator based schemes.

In order to classify the accumulator-based and the MISR response compaction schemes we compute the arithmetic mean of the results of Tables 1, 2, 3, 4 and 6 for each response compaction scheme. A graphical representation of the results is given in Figure 6. We conclude that the proposed response compaction scheme is the best accumulator based scheme and its performance is close to the performance of MISRs.

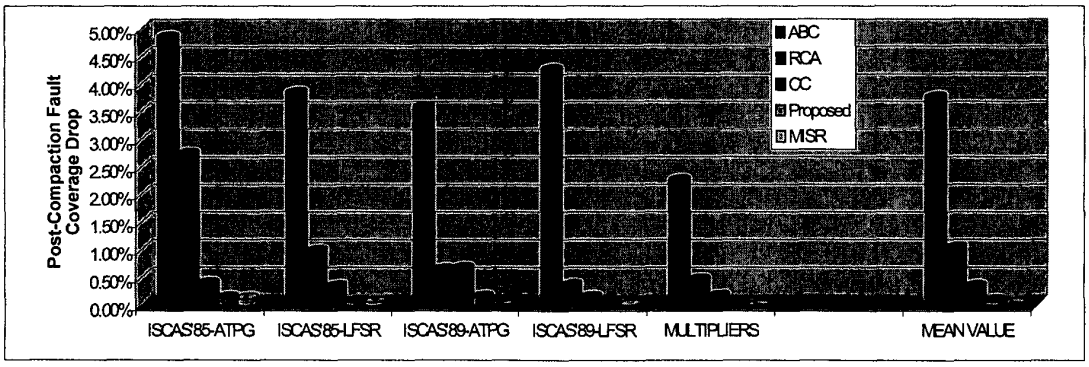

Figure 6: A classification of the test response compaction schemes

5. Conclusion

In this paper we show that an accumulator modified to behave as a non-linear feedback shift register is suitable for test response compaction. The hardware required for the modification is less than that required to modify a register to a MISR. Experimental results on ISCAS'85 benchmark circuits, ISCAS'89 benchmark circuits and various types of multipliers show that the proposed scheme obtains higher post-compaction fault coverage than the already known accumulator-based schemes and comparable to that achieved using a MISR.

A theoretical analysis of the aliasing probability is currently under consideration. As future work we can refer to the use of the proposed scheme, the accumulator behaving as a non-linear feedback shift register, for test pattern generation.

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