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Σεμινάριο στην τεχνολογία των memristors

Ημερομηνία: 9 Σεπτεμβρίου 2024 και ώρα 15:00-17:00

Τοποθεσία: Αίθουσα Σεμιναρίων, Τμήμα Μηχανικών Η/Υ και Πληροφορικής

Συντονιστής: Β. Τενέντες, Επίκουρος Καθηγητής ΤΜΗΥΠ, ΠΙ

15:00-15:45: The fourth element (or the rediscovered memristor)

Ομιλητής: Valeri Mladenov

Professor at the Technical University of Sofia, Bulgaria

Abstract: Memristor is the fourth fundamental circuit element which was predicted in the 1970s and rediscovered in HP labs in 2008. The HP memristor, is constructed using a nanometer scale TiO2 thin-film that comprises a doped and an undoped region. It is a novel circuit element with very good memory and switching properties, nano-size dimensions, low power consumption, and good compatibility with complementary metal oxide semiconductor (CMOS) integrated circuits. The potential applications of memristors are not only limited to artificial biological systems and nonvolatile RAM, but also extend to reconfigurable nanoelectronics. Furthermore, memristors introduce novel paradigms in the application-specific integrated circuits (ICs) and field-programmable gate arrays (FPGAs) domains. The implementation of memristors in ICs offers unprecedented memory capacity and device density while occupying a significantly smaller area. Memristors could be used for energy-efficient storing and processing information in high-density integrated chips applicable in nonvolatile memories, artificial neural networks, and neuromorphic computing circuits. In this lecture, an introduction to memristors is given, along with the presentation of mathematical and SPICE models for these devices. Additionally, an overview of the potential applications of memristors is provided.

15:45-16:00 Διάλειμμα

16:00-16:30: Memristor-Based Classical Neural Network Implementations with Adjustable Synaptic Weights

Ομιλητής: Georgi Tsenov

Associate Professor at the Technical University of Sofia, Bulgaria

Abstract: The memristors are innovative electronic elements with nano-sized structure and with very good memory and switching abilities. They have very low power consumption and a good compatibility to CMOS integrated chips, and they could be used in neural networks, memories, and many other schematics. Most of the memristor implementations are with crossbar configuration, suitable for CNNs, but recently chips with 8, 16 or 32 individually accessible memristors was released by Knowm, providing the option to build classical neural network designs. A classical artificial neural network can be implemented as hardware analog device with memristor-based synapses that can be tuned to certain scaled resistance levels, opening the option for analog computing and neural network coefficient reprogramming. In this network, each synapse is realized with only one memristor, thus providing a higher reduction in circuit complexity and with main benefit of that individual memristor resistance value can be adjusted with external control voltage signals. The summing and scaling component implementations are based on op-amps and memristors. We use the most common hardlim or logarithmic-sigmoidal activation function and it is realized by a voltage-controlled source. The operation of the proposed memristor neural network is analyzed and simulated in both LTSPICE and MATLAB, and the derived results are compared and verified successfully with hardware implementations on breadboards. The proposed memristor-based neural network is a significant step for engineering low power complex networks in very high-density integrated circuits and chips.

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16:30-17:00: Automatic SPICE memristor model estimation based on measurement data from existing memristors

Speaker: Georgi Tsenov

Associate Professor at the Technical University of Sofia, Bulgaria

Abstract: The real-world production memristor devices produce a modelling challenge due to having a memristor element variance and henceforth a measured difference between breadboard made circuits and LTSPICE or MATLAB simulated circuits with classical models, resulting in a variance owed to the difference in existing memristor models and the real world hardware. When a new memristor device is studied usually no model is provided and it is useful if there is a tool that automatically can update existing models with the production memristor parameters. This motivated us to implement a procedure realized in MATLAB that takes real world measured data, approximates the memristor parameters and provides a MATLAB and LTSPICE models that are precise representation of the real world memristor device.

Σύντομα βιογραφικά των ομιλητών:

Dr. Valeri Mladenov received his Ph.D. from the Technical University of Sofia (TU Sofia), Bulgaria in 1993. In 2019 he defenses a “Doctor of Sciences” thesis at the same institution. In 2004 he becomes the head of the department Fundamentals of Electrical Engineering. Since June 2011 he was a Dean of Faculty of Automatics, since Dec. 2011 he has been a Vice-Rector of TU Sofia. Currently, he is Head of the Department of Fundamentals of Electrical Engineering and Head of the Neurocomputing laboratory of TU-Sofia. He is a guest lecturer at the Faculty of Electrical Engineering, Eindhoven University of Technology, in the Netherlands, and many others. Prof. Mladenov’s research interests are in the field of electrical engineering, artificial intelligence, power systems, electronics, neural networks. He has received many international research fellowships. He has more than 350 scientific papers in professional journals and conferences. He is a co-author of twenty books and manuals for students. He had received many research grants and also with his team he participated and participate in many national and international projects - H2020, FP7, Royal Society, DFG, NWO, Erasmus+, and others. As a member of several editorial boards, Prof. Mladenov serves as an editor in chief, associate editor, and reviewer for a number of professional journals and conferences. He is a Senior Member of IEEE, a member of the IEEE Circuit and Systems Technical Committee (TC) on Cellular Nonlinear Networks and Memristor Array Computing (CNN- MAC), and an Educational Activities Officer of the Bulgarian IEEE section. He is also a Senior Member of the International Neural Networks Society (INNS), Member of the International Council of Large Electric Systems, (SIGRE), member of the Steering Committee of the International Symposium on Theoretical Electrical Engineering (ISTET), member of the Management Boards of the Scientific and Technical Union of the Power Engineers, and the Union of Automation and Informatics in Bulgaria.

Dr. Georgi Tsenov is currently an Associate Professor at Fundamentals of Electrical Engineering Department of the Automation of Technical University of Sofia. He is an IEEE member and member of Bulgarian chapter of CAS. He is member of Cellular Nanoscale Networks and Array Computing Technical Committee (CNNAC-TC). He is a member of the council of Faculty of Automation in Technical University – Sofia.