# A Totally Self-Checking Error Correcting/Detecting Circuit for a Class of SEC/DED/AUED Codes

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## Abstract

Single Error Correcting, Double Error Detecting and All Unidirectional Error Detecting (SEC/DED/AUED) codes are especially useful in computer systems because they are effective against the errors caused by transient, intermittent and permanent faults. In this paper we give the design of a TSC Error Correcting/Detecting circuit for the SEC/DED/AUED codes given in [4]. Since the information length is usually a power of two only SEC/DED/AUED codes with 4, 8, 16, 32, ... information bits are considered. The proposed circuit is the first known TSC Error Correcting/Detecting Circuit for SEC/DED/AUED codes.

## I. Introduction.

A very large number of t-Error Correcting/(t+1)-Error Detecting and All Unidirectional Error Detecting (t-EC/(t+1)-ED/AUED) codes have been proposed in the open literature [1-8]. The reason is that the t-EC/(t+1)-ED/AUED codes are especially useful in computer systems due to their effectiveness against the errors caused by transient, intermittent and permanent faults [1, 2].

Apart from the effectiveness of an error control code in combating errors, its suitability for use in a computer system heavily depends on the existence of simple and fast encoder and decoder circuits [1, 10]. Unless the hardware needed to generate and check the code is relatively simple compared to the hardware monitored, a fault-prone decoder could increase rather than decrease the likelihood of erroneous information propagation. Also even a delay of one microsecond in handling critical-path information in a computer could be intolerable. Unfortunately, both the decoder complexity and the decoding delay tend to increase rapidly with the number of errors to be corrected [10]. In practice we correct a very small number of errors, usually one, in order to keep the decoder complexity low and the decoding delay small. Thus among the t-EC/(t+1)-ED/AUED codes the SEC/DED/AUED codes seems that will find the most wide range of applications.

Besides the above a major concern in the implementation of a code is to ensure that the error correcting/detecting circuit achieves the TSC goal. In this case the TSC goal means that the first erroneous input of the error D/C circuit that exceeds the error correction capabilities of the code is signaled by the circuit. A method to achieve this is the use of Totally Self-Checking (TSC) circuits. The concept of the TSC circuits has been introduced in [11, 12] and formally defined in [12] as the circuit which is self testing and fault secure.

**Definition 1.** A circuit is self-testing for a set of faults F if, for every fault in F, the circuit produces a noncode output for at least one code input.

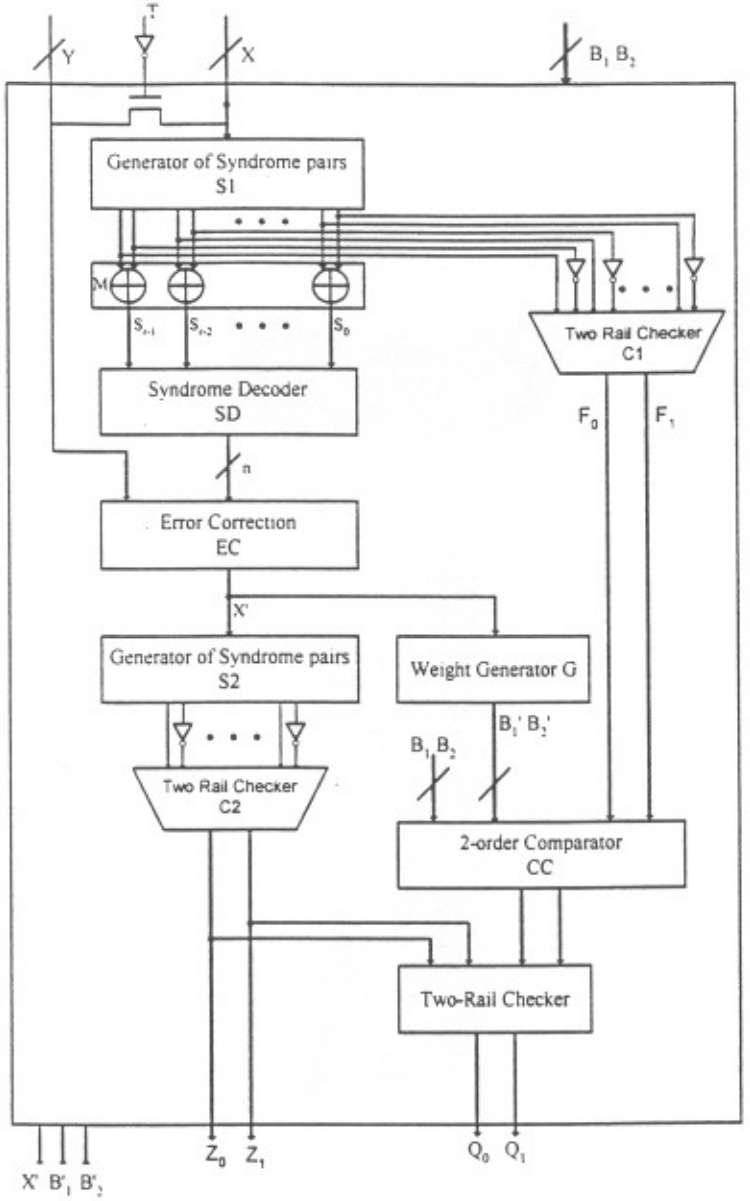


**Figure 1. A TSC Error Correcting/Detecting circuit for SEC/DED/AUED codes**

**Definition 2.** A circuit is fault secure for a set of faults F if, for every fault in F, the circuit never produces an incorrect code output for all code inputs.

In this work we give the design of a TSC Error C/D circuit for the SEC/DED/AUED codes proposed in [4]. The fault model considered is the single stuck-at fault model.

## II. Design Method

The design of a systematic SEC/DED/AUED code starts from a single error correcting parity check code with minimum Hamming distance equal to 3 and appends to each code word X of the parity check code a suitable check symbol which depends on the Hamming weight of X. Taking into account that the information length k is usually a power of two, only SEC/DED/AUED codes with k= 4, 8, 16, 32, ... will be considered.

At first we will show that the circuit of figure 1 during its fault free operation is an Error C/D circuit for SEC/DED/AUED codes. The 2nd order comparator is defined as a circuit that compares two operands and decides if they differ in less than 2 bit positions. When the outputs $Q_0$, $Q_1$ are two-rail encoded the output $X'B_1'B_2'$ is the correct code word while if $Q_0=Q_1$ an only detectable error has occurred in the received word. We consider various cases.

a. The circuit receives an error free word, that is a code word of the SEC/DED/AUED code. Then it is evident that the outputs of the two rail checkers C1 and C2 are two rail encoded and $B_1'B_2'=B_1B_2$, thus the outputs $Q_0$, $Q_1$ are two-rail encoded.

b. The received word has been corrupted by a single error. In this case $F_0=F_1$, the error is corrected in the Error Correction module, thus the output of C2 will be two-rail encoded and $B_1'B_2'=B_1B_2$. Then the output of the 2-order comparator will be two-rail encoded as well as the outputs $Q_0$, $Q_1$.

c. The received word has been corrupted by a double error. In this case we examine three subcases:

c.1. One error has occurred in X part and the other in $B_1B_2$ part of the received word. Then $F_0=F_1$ and $D(B_1B_2 \oplus B_1'B_2')=1$, thus the output of the 2-order comparator is not two-rail encoded and $Q_0=Q_1$, therefore the error is detected.

c.2. Both errors have occurred in the X part of the received word. A double error in the X part is always detectable by the Hamming code. We examine two subcases

i. The syndrome is equivalent to the syndrome of a single error in one of the bits of X. Then the single error is corrected. $F_0=F_1$ and $D(B_1B_2 \oplus B_1'B_2')\geq 1$, therefore $Q_0=Q_1$ and the error is detected.

ii. The syndrome is not equivalent to a single error in one of the bits of X. Then none error is corrected and $Z_0=Z_1$, therefore $Q_0=Q_1$ and the error is detected.

c.3. Both errors have occurred in the $B_1B_2$ part of the received word. Then $D(B_1B_2 \oplus B_1'B_2')=2$ and the error is detected.

d. A unidirectional error with multiplicity greater than 2 has occurred. In the same way we can prove that the error is detected.

Among the Hamming codes that will be used in this paper for the construction of a SEC/DED/AUED code, only the Hamming code with k=4 is a complete code. For k= 8, 16, 32, ... shortened Hamming codes should be used. To achieve the design of a TSC Error D/C circuit for SEC/DED/AUED codes we will show that the all ones vector must belong to the code words of the Hamming code. The all ones code word always belong to the code words of a complete Hamming code while in a shortened Hamming code it depends on the chosen parity check matrix. Let k' and k be respectively the number of information bits of the complete and shortened Hamming code with r check bits.

**Lemma 1.** Let H be the parity check matrix of the shortened Hamming code C. The all ones vector will be one of the codewords of C if and only if each row of H has an even number of ones.

The proof is evident.

**Table 1**

| r | k' | k | k'-k |
|---|---|---|---|
| 3 | 4 | 4 | 0 |
| 4 | 11 | 8 | 3 |
| 5 | 26 | 16 | 10 |
| 6 | 57 | 32 | 15 |
| 7 | 120 | 64 | 56 |

Let C be the shortened Hamming code that is derived by removing a specific set of s columns of the parity check matrix of the complete Hamming code C', and M the matrix with columns the above mentioned s columns. Then taking into account that all the rows of the parity check matrix of the complete Hamming code have even number of ones and Lemma 1 we conclude that each row of M must have an even number of ones.

Table 1 presents the number of check bits r for k information bits with k= 8, 16, 32 and 64, as well as the number of the columns k'-k of the complete Hamming code parity check matrix that must be canceled in order to take the corresponding shortened code. For example if we remove from the parity check matrix of the complete Hamming code with 11 information bits the columns

$$M_1=\begin{bmatrix}0&1&1\\1&0&1\\1&0&1\\0&1&1\end{bmatrix} \text{ or } M_2=\begin{bmatrix}0&1&1\\0&1&1\\1&0&1\\1&1&0\end{bmatrix} \text{ or } M_3=\begin{bmatrix}1&0&1\\0&1&1\\1&1&0\\0&1&1\end{bmatrix}$$

we get a shortened Hamming code with k=8 which includes the all ones vector among its code words. As another example if we remove from the parity check matrix of the complete Hamming code with 26 information bits the columns that constitute the 3-out-of-5 code we get a shortened Hamming code with 16 information bits which includes the all ones vector among its code words.

We consider that the code input space of the circuit of figure 1 consists of all the code words of the SEC/DED/AUED code as well as all the code words of the SEC/DED/AUED code corrupted by a single error. Let n be the length of the Hamming code and r the number of the check bits.

The syndrome generator S1 consists of r parity checkers. When S1 receives as inputs the code words of the SEC/DED/AUED code each parity checker receives all possible code input vectors and thus is self-testing. This is valid independent of the parity check matrix of the Hamming SEC code that has been used for the construction of the SEC/DED/AUED code. The syndrome generator S2 is identical to S1. When the circuit of figure 1 receives code words of the SEC/DED/AUED code and the modules M, SD and EC are fault free, S2 receives the same code inputs as S1. Therefore each parity checker of

S2 receives all possible code input vectors and thus is self-testing.

Two rail checker C1 has been implemented as a tree of 2-pair input two-rail checker modules. For k= 4, 8, 16, 32, ... each module receives, during normal fault free and error free operation, its test set.

When the Error C/D circuit receives code words of the SEC/DED/AUED code and the modules M, SD, EC and S2 are fault free then the module C2 receives the input vectors that C1 receives, therefore C2 receives its test set.

When the Error C/D circuit, fig. 1, receives code words of the SEC/DED/AUED code each XOR gate of module M receives the inputs (0,0) and (1,1). When the Error C/D circuit receives as inputs code words corrupted by single errors then each XOR gate of M receives the inputs (0,1) and (1,0). The above implies that each XOR gate of M is tested exhaustively.

The syndrome decoder circuit (SD) is an r to n decoder ( the output corresponding to the all zeros input as well as the outputs n+1 to $2^r$-1 have been eliminated).When the modules S1 and M are fault free and the Error C/D circuit receives code words of the SEC/DED/AUED code uncorrupted by errors the syndrome decoder receives only the all-zeros vector. When the Error C/D circuit receives code words corrupted by single errors then the module SD receives n of all $2^r$ possible input vectors and the majority of stuck-at faults are tested. However, there exist a small number of stuck-at faults that are undetectable. These faults will be detected by a self exercising mechanism which will be presented further down.

The error correcting circuit EC consists of a row of two-input XOR gates. The i XOR gate takes as inputs the i bit of the received word and the i output line of the decoder. When the modules S1, M and SD are fault free and the Error C/D circuit receives code words of the SEC/DED/AUED code uncorrupted from errors, then each XOR gate of the module EC receives respectively the inputs (0,0) and (0,1). When the Error C/D circuit receives code words corrupted by single errors and the modules S1, M and SD are fault free then each XOR gate of EC receives the rest inputs (1, 0) and (1, 1). Therefore each XOR is tested exhaustively.

The weight generator is designed as proposed in [14] and during normal fault and error free operation, each module receives all possible inputs, thus it is self testing. The all ones vector is necessary so that the full adder or half adder module with the maximum weight to receive all possible input vectors.

Hints for designing TSC second order comparators have been given in [12]. In our design the second order comparator is an embedded circuit that has been designed to receive, during the normal fault free and error free operation, its test set, thus it is self testing.

It is easy to show that an error at the output of a module of the proposed Error C/D circuit propagates to the primary outputs of the circuit. Also it is easy to show that the Error C/D circuit is fault secure.

As we have seen the majority of the stuck-at faults is detected when the Error C/D Circuit receives as input code words of the SEC/DED/AUED code. However there exist some stuck-at faults in the modules M, SD and EC ( we have already refer to them) that are detected only when the Error C/D Circuit receives as inputs code words of the SEC/DED/AUED code corrupted by single errors. There exist also some stuck-at faults in SD that are not detected by codewords corrupted by single errors. It is well known that in a well designed system the probability the Error C/D circuit to receive a code word corrupted by a single error is enough smaller than the probability to receive an error free code word. To avoid the accumulation of undetected faults we use a Built-In self-exercising mechanism for periodic testing. The only additional circuit that is required is a shift register with length equal to $2^r$-1 and r XOR trees. Figure 2 presents the shift register and the r XOR trees for the case that k=8 and the shortened Hamming code has been derived eliminating from the complete Hamming code parity matrix the columns of matrix $M_1$. The inputs $Y=(Y_{11}Y_{10}Y_9Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1)$ of the Error C/D circuit are driven by the outputs $Z_{14}Z_{13}Z_{12}Z_{11}Z_{10}Z_8Z_7Z_5Z_4Z_3Z_2Z_1$ of the shift register, while the inputs $X=(X_{11}X_{10}X_9X_8X_7X_6X_5X_4X_3X_2X_1)$ are driven by the outputs $Z_{14}Z_{13}Z_{12}Z_{11}Z_{10}P_8Z_7Z_5P_4Z_3P_2P_1$. $2(2^r-1)$ vectors are enough for testing the single stuck-at faults which are not tested when the Error C/D circuit receives only code words of the Hamming code. The $2(2^r-1)$ vectors are generated by shifting $2^r$-1 times each one of two vectors that are placed in the shift register using the set and reset asynchronous inputs of the flip flops. The two vectors have Hamming weight (number of ones) equal to one and $2^r$-2 respectively. While during the normal operation of the Error C/D circuit the outputs $Q_0$, $Q_1$ determine whether the output $X'B_1'B_2'$ of the circuit is a code word of the SEC/DED/AUED code or not, during the test mode the outputs $Z_0$, $Z_1$ determine if one of the predefined stuck-at faults have occurred in the Error C/D circuit. Specifically if $Z_0=Z_1$ a stuck-at fault has occurred in the circuit.

The circuit proposed in this work is the first known TSC Error Correcting/Detecting Circuit for SEC/DED/AUED codes.

## Conclusion

A TSC Error C/D circuit for a class of SED/DED/AUED Codes has been given for all practical cases with 4, 8, 16, 32, ... information bits. The accumulation of some faults that are not detected or is less

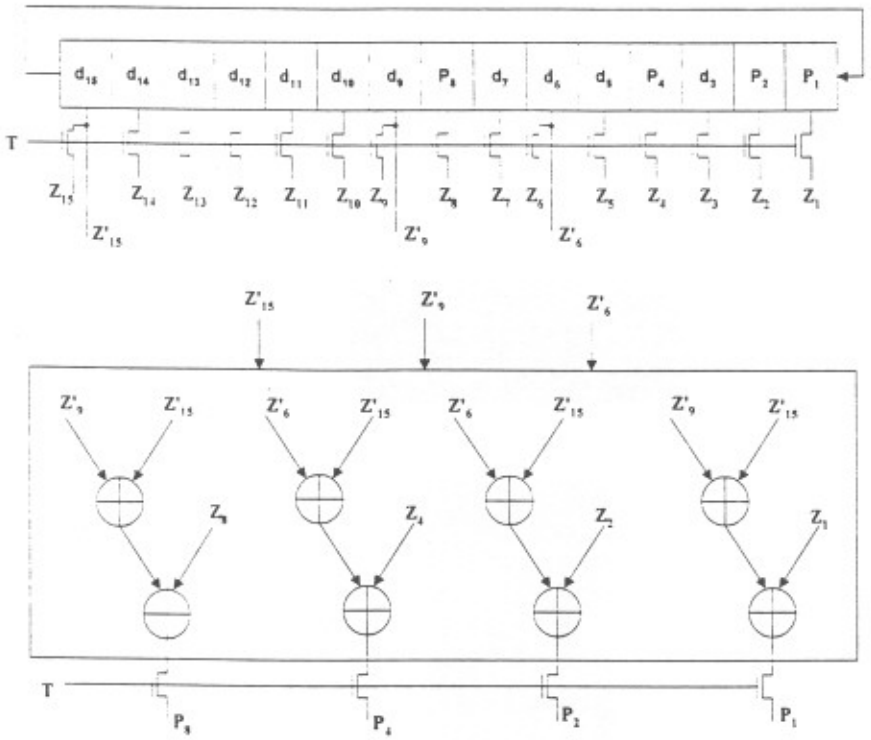

**Figure 2. Test Pattern generation mechanism**

possible to be detected during the normal operation of the circuit is avoided by using a self exercising mechanism in a test mode. The proposed circuit is the first TSC Error C/D circuit for SEC/DED/AUED codes.

## References


[1] D. K. Pradhan and J. J. Stiffler, "Error-correcting codes and self-checking circuits", IEEE Comput. Mag., Vol. 13, pp. 27-37, Mar. 1980.

[2] D. K. Pradhan, "A new class of error correcting/detecting codes for fault tolerant computer applications", IEEE Trans. Comput., vol. c-29, pp. 471-481, June 1980.

[3] B. Bose and D.K. Pradhan, "Optimal unidirectional error detecting correcting codes", IEEE Trans. Comput., Vol.C-31, pp.564-568, June 1982.

[4] D. Nikolos, N. Gaitanis and G. Philokyprou, "Systematic t-Error Correcting/All Unidirectional Error Detecting Codes", IEEE Trans. on Comput. Vol. C-35, No. 5, May 1986, pp. 394-402.

[5] M. Blaum and H.V. Tilborg, "On t-Error Correcting/All Unidirectional Error Detecting Codes", IEEE Trans. Comp. Nov. 1989, pp. 1493-1501.

[6] T.R.N. Rao, E. Fujiwara, "Error-Control coding for computer systems." Prentice-Hall International, 1989.

[7] D. Nikolos, "Theory and Design of t-Error Correcting/d-Error Detecting (t<d) and All Unidirectional Error Detecting Codes." IEEE Trans. Comp., Feb. 1991, pp.132-142.

[8] M. Blaum ed., Codes for Detecting and Correcting Unidirectional Errors", IEEE Computer Society Press, 1993.

[9] E. Fujiwara and Pradhan, "Error Control Coding in Computers", IEEE Comput. Mag., pp. 63-72, July 1990.

[10] J. J. Stiffler, "Coding for Random-Access Memories", IEEE Trans. Comput., vol. 27, pp. 526-531.

[11] W. C. Carter and P. F. Schneider, "Design of dynamically checked computers", in Proc. 4th Cong. IFIP, Edinburgh, Scotland, vol. 2, pp. 878-883, Aug. 5-10, 1968.

[12] D. A. Anderson, "Design of self-checking networks using coding techniques", Coord. Sci. Lab., Univ. Illinois, Urbana, IL, Tech. Rep. R-527, 1971.

[13] N. Gaitanis, "The Design of TSC Error C/D Circuits for SEC/DED Codes", IEEE Trans. Comput., vol. 37, March 1988, pp. 258-265.

[14] A. Paschalis, D. Nikolos and C. Halatsis "Efficient modular design of TSC checkers for m-out-of 2m codes", IEEE Trans. Comput., vol. 37, pp. 301-309, March 1988.